The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended) A circuit comprising:
a first supply voltage port;
a second supply voltage port;
a current mirror circuit comprising a first current mirror port and a second current mirror port, the second current mirror port for propagating an input current from the first supply voltage port to the second supply voltage port through the current mirror circuit coupled there between, where the first current mirror port is for providing N times the input current; [[and,]]
a current ratioing circuit comprising a first portion disposed between the first current mirror port and the second supply voltage port and a second portion disposed between the first supply voltage port and the second supply voltage port, the second portion comprising a load current path, where the current ratioing circuit is for propagating M times N times the input current through the load current path,
wherein the first portion of the current ratioing circuit comprises a first bipolar transistor having a first base terminal and one of a first collector terminal and first emitter terminal coupled with the first current mirror port and the other of the first emitter terminal and the first collector terminal thereof coupled with the second supply voltage port, and
wherein the second portion of the current ratioing circuit comprises a second bipolar transistor having a second base terminal coupled with the first base terminal and one of a second collector terminal and second emitter terminal coupled to the load current path and the other of the second emitter terminal and the second collector terminal thereof coupled with the second supply voltage port, wherein the second bipolar transistor is M times larger than the first bipolar transistor;
a current path disposed between the first supply voltage port and the coupled first and second base terminals for propagating current therein in response to the input current; and
wherein at least one of N and M is other than 1.

2. (original) A circuit according to claim 1 comprising a current sink coupled between the second supply voltage port and the second current mirror port for sinking the input current through the current mirror circuit from the second current mirror port to the second supply voltage port.

3. (cancelled)

4. (original) A circuit according to claim 1 wherein each of N and M are other than 1.

5. (original) A circuit according to claim 1wherein the second portion of the current ratioing circuit comprises a plurality of second bipolar transistors having a plurality of second base terminals coupled with the first base terminal and one of a plurality of second collector terminals and a plurality of second emitter terminals coupled to the load current path and the other of the plurality of second emitter terminals and the plurality of second collector terminals thereof coupled with the second supply voltage port, wherein the plurality of second bipolar transistors disposed together in parallel are M times larger than the first bipolar transistor.

6. (cancelled)

7. (currently amended) A circuit according to claim 1 wherein the current path comprises a first [[third]] field effect transistor (FET) having a first [[third]] gate terminal, a first [[third]] drain terminal and a first [[third]] source terminal disposed in series along the current path, the first [[third]] gate terminal coupled with the second current mirror port for controlling propagation of the current between the first [[third]] source and drain terminals in dependence upon the input current.

8. (currently amended) A circuit according to claim 1 wherein the current mirror circuit further comprises:

a second FET having a second gate terminal, a second drain terminal and a second source terminal, the second source and second drain terminals disposed in series between the first supply voltage port and the second current mirror port, a source of the second FET one of coupled to or [[and]] resistively coupled to the first base terminal.

9. (currently amended) A circuit according to claim 8 wherein the current mirror circuit further comprises:
a third [[first]] FET having a third [[first]] gate terminal, a third [[first]] drain terminal and a third [[first]] source terminal, the third [[first]] source and third [[first]] drain terminals disposed in series between the first supply voltage port and the first current mirror port with one of the third [[first]] drain and third [[first]] source terminals coupled with the third [[first]] gate terminal,
wherein the third [[first]] FET is N times wider than the second FET.

10. (currently amended) A circuit according to claim 9 wherein at least one of the first FET, [[and]] the second FET, and the third FET are PFETs.

11. (currently amended) A circuit according to claim 2 comprising a first ~~second~~ current source coupled to the first and second base terminals of the first and second bipolar transistors for providing an offset current thereto.

12. (original) A circuit according to claim 11 wherein, in use of the circuit, a potential difference is realized between the second collector and second emitter terminals of the second bipolar transistor of approximately 300-400mV in response to the offset current.

13. (currently amended) A circuit according to claim 7 comprising a loop stabilization circuit comprising a first capacitor disposed between the third drain ~~source~~ and third gate terminals of the third FET; and,
a first ~~second~~ resistor disposed between the third drain terminal of the third FET and coupled to a node formed between the first and second base terminals of the first and second bipolar transistors.

14. (currently amended) A circuit according to claim 13 comprising second and third ~~third and fourth~~ resistors disposed between the first base terminal and the node and the second base terminal and the node, respectively.

15. (original) A circuit according to claim 11 comprising a RF input port formed at the second base terminal of the second bipolar transistor for receiving of a RF input signal.

16. (original) A circuit according to claim 7 wherein the load current path comprises a differential amplification stage disposed in series between the first supply voltage port and one of the second collector and second emitter terminals of the second bipolar transistor.

17. (original) A circuit according to claim 16 wherein the differential amplification stage comprises:
first and second bias ports coupled to one of the third drain and third source terminals of the third FET;
a differential bias port coupled to one of the second collector and second emitter terminals of the second bipolar transistor;
a first RF signal input port for receiving a first RF input signal; and,
a second RF signal input port for receiving of a second RF input signal, where the first and second RF signal input ports are for, in combination, receiving of a differential RF input signal.

18.-20. (cancelled)